Amendments to the Claims:

The following listing of claims will replace all prior versions and listing of claims:

1. (original) A method of fabricating an integrated circuit device comprising:

depositing a composite etching stop layer overlying a metal line in a substrate wherein said composite etching stop layer comprises a TEOS oxide layer overlying an etching stop layer;

depositing a dielectric layer overlying said composite etching stop layer;

etching an opening through said dielectric layer stopping at said composite etching stop layer;

thereafter removing said composite stop layer within said opening; and

filling said opening with a conducting layer to complete said fabrication of said integrated circuit device.

2-26. (cancelled).

27. (new) An integrated circuit device comprising:

a composite etching stop layer overlying a metal line in a substrate wherein said composite etching stop layer comprises a TEOS oxide layer overlying an etching stop layer;

a dielectric layer overlying said composite etching stop layer; and

a conducting layer lying in an opening through said dielectric layer and said composite etching stop layer to said metal line.

28. (new) The device according to Claim 27 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions and metallization formed in and on a silicon substrate.

29. (new) The device according to Claim 27 wherein said composite etching stop layer comprises:

said etching stop layer selected from the group consisting of: silicon carbide, silicon nitride, SiCN, SiOC, SiOCN, and p-BCB; and

said TEOS oxide layer overlying said etching stop layer wherein said TEOS oxide layer provides moisture resistance to said composite etching stop layer.

30. (new) The device according to Claim 27 wherein said composite etching stop layer has a thickness of between about 300 and 1000 Angstroms.

31. (new) The device according to Claim 27 wherein said etching stop layer has a thickness of between about 200 and 600 Angstroms.

32. (new) The device according to Claim 29 wherein said TEOS oxide layer has a thickness of between about 150 and 500 Angstroms.

33. (new) The device according to Claim 27 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.

34. (new) A composite etching stop layer comprising:

an etching stop layer on a copper line in a substrate wherein said etching stop layer is selected from the group consisting of: silicon carbide, silicon nitride, SiCN, SiOC, SiOCN, and p-BCB; and

a TEOS oxide layer overlying said etching stop layer.

35. (new) The device according to Claim 34 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions formed in and on a silicon substrate.

36. (new) The device according to Claim 34 wherein said composite etching stop layer has a thickness of between about 300 to 1000 Angstroms.

37. (new) The device according to Claim 34 wherein said etching stop layer has a thickness of between about 200 and 600 Angstroms.

38. (new) The device according to Claim 34 wherein said TEOS oxide layer has a thickness of between about 150 to 500 Angstroms.

39. (new) The device according to Claim 34 further comprising:

a dielectric layer overlying said composite etching stop layer; and

a conducting layer in an opening in said dielectric layer and said composite etching stop layer to said copper line.

40. (new) The device according to Claim 39 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.

41. (new) An integrated circuit device comprising:

a composite etching stop layer overlying a copper line in a substrate wherein said composite etching stop layer comprises:

a silicate carbide etching stop layer; and

a TEOS oxide layer overlying said silicon carbide etching stop layer;

a dielectric layer overlying said composite etching stop layer; and

a conducting layer filling an opening in said dielectric layer and said composite etching stop layer to said copper line.

42. (new) The device according to Claim 41 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions formed in and on a silicon substrate.

43. (new) The device according to Claim 41 wherein said composite etching stop layer has a thickness of between about 300 to 1000 Angstroms.

44. (new) The device according to Claim 41 wherein said silicon carbide etching stop layer has a thickness of between about 200 and 600 Angstroms.

45. (new) The device according to Claim 41 wherein said TEOS oxide layer has a thickness of between about 150 to 500 Angstroms.

46. (new) The device according to Claim 41 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.